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10EE764

Seventh Semester B.E. Degree Examination, July/August 2021
VLSI Circuits and Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. With the help of necessary structures, explain the p-well CMOS fabrication process. **(10 Marks)**

b. With graphical representation, explain the speed/power performance of available IC technologies. **(05 Marks)**

c. Outline the procedure for making E-beam mask. Mention different type of E-bean mask. **(05 Marks)**

2 a. Discuss drain to source current versus voltage relationship for non-saturated and saturated regions. **(10 Marks)**

b. Explain the Latch-up phenomena in CMOS circuits. **(05 Marks)**

c. Draw an n-MOS transistor circuit model showing different capacitances. **(05 Marks)**

3 a. Draw the stick diagram and symbolic diagram for a simple nwell based BiCMOS inverters. **(06 Marks)**

b. List the colour, stick encoding, layers, mask layout encoding, CIF layers for a simple metal nMOS process. **(10 Marks)**

c. Draw mono chrome stick diagram of C-MOS inverter. **(04 Marks)**

4 a. Obtain the expression for total delay for N-stages of nMOS and CMOS invertors interms of width factor and delay. **(10 Marks)**

b. What is sheet resistance? Calculate sheet resistance of transistor channel L = 8λ, w = 2λ if n transistor channel $R_s = 10^4$ Ω/square. **(05 Marks)**

c. Write short note on BiCMOS drivers. **(05 Marks)**

5 a. With neat diagram, explain the concept of scaling in nMOS transistor. **(05 Marks)**

b. Obtain scaling factor for the following parameters :

i) Gate capacitance C_g
ii) Current density
iii) Gate delay
iv) Channel resistance
v) Saturation current. **(10 Marks)**

c. How the propagation delay can be estimated for a typical metal interconnection model. **(05 Marks)**

6 a. Explain the concept of dynamic CMOS logic. **(06 Marks)**

b. Explain structured design approach for a parity generator circuit. Draw the NMOS stick diagram of its basic cell. **(08 Marks)**

c. Explain the concept of a general logic function block. **(06 Marks)**

7 a. Explain with neat diagram 4 × 4 barrel shifter. **(10 Marks)**

b. Explain design of an ALU subsystem for design of 4 – bit adder. **(10 Marks)**

8 Write short notes :

a. Super buffers
b. Regularity
c. Some general consideration
d. Pseudo-nMOS logic. **(20 Marks)**

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